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Ultra-low-latency 10Gbit/s Ethernet MAC

CT1009-XGMAC - Product Brief - Version 1.2 – 06 Dec 2014

Introduction

The Chevin Technology XGMAC is an IP block which simplifies the FPGA integration of Ultra low-latency 10Gbit/s Ethernet connectivity in Xilinx and Altera FPGAs.

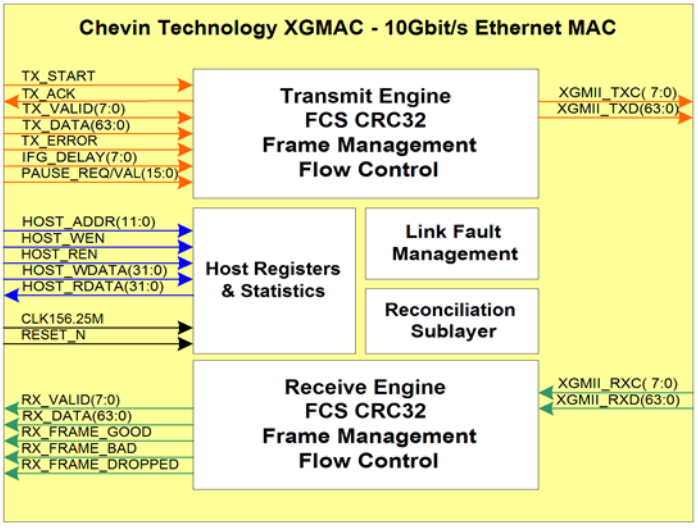
The block can be used directly with an external or internal PHY using Chevin Technology XGPHY for the lowest possible latency.

The application side can be driven by any logic that generates and decodes Ethernet frames. The MAC manages frame timing, CRC32 Checksum insertion and generation, and manages the lower layer fault handling and XGMII interface coding.

Flow control provides back pressure to peer node and is handled automatically by the MAC in both directions independently.

A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for different frame sizes, types and checksum errors.

Get up and running quickly with the reference design on a Xilinx KC705 development board and a simple “ping” command line with the ICMP/ARP options. Use standard software TCP/UDP tools when integrated with the XGTCP IP block from Chevin Technology’s portfolio of IP blocks.



Key Features

- Designed to IEEE 802.3-2008 Specification
- Low Latency TX 32ns RX19ns
- Integrated FCS CRC32 check/generate
- Small Footprint 2k1 ALMs, 3k2 LUTs
- Flow Control option with Pause packets
- Programmable max frame length
- Reconciliation Layer -Local /Remote Faults
- Programmable Inter Frame Gap
- Deficit Idle Count for maximum throughput
- Cut-through mode for lowest latency
- Store-and-forward for minimum app load
- MAC address filtering options
- Detailed traffic analysis statistics collection
- Optional MDIO master for controlling PHY

“Drop the XGMAC IP Block into your Xilinx or Altera FPGA design for extremely fast and consistent Low-latency Ethernet connectivity”

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

Chevin Technology XGMAC

Integration in FPGA

A simple host interface allows control and configuration of the XGMAC registers and statistics block. The reference design includes a UART host interface port and example host software to drive this interface and can be used to speed up integration work.

The 64bit XGMII interface connects directly to any XGMII compatible PHY preferably utilizing Kintex, Virtex and Stratix devices' 10Gbit capable SerDes (Multi Gigabit Transceivers) that provide the lowest latency, power, board size and cost, and the best overall performance.
We recommend pairing the XGMAC with Chevin Technology's XGPHY, an ultra-low-latency 10GBASE-R block for SFP+ Direct Attach copper cable or SR/LR Fiber connection.

The application side connects directly to user logic which can be user logic FIFOs to AXI4 or Avalon standard interfaces or shared via an arbiter to other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more Integrated FPGA solution.

Deliverables

- RTL VHDL source code
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Design on Xilinx KC705 development board
- Simulation Test bench
- Build scripts for ISE/Vivado
- Support for integration into FPGA

Latency Figures

Lowest latency is achieved by using the cut-through mode. In this mode the MAC starts out-putting payload data while the frame is still in transit. Once the FCS field arrives the checksum can be calculated and the application is notified of pass/fail. Store-and-forward mode avoids this by completely ingesting a frame before checking the FCS field.

Last FCS byte input at XGMII interface to CRC32 checksum result valid **32ns**

Preamble byte input at XGMII interface to the first data payload byte at application **19ns**

FPGA Resource Figures

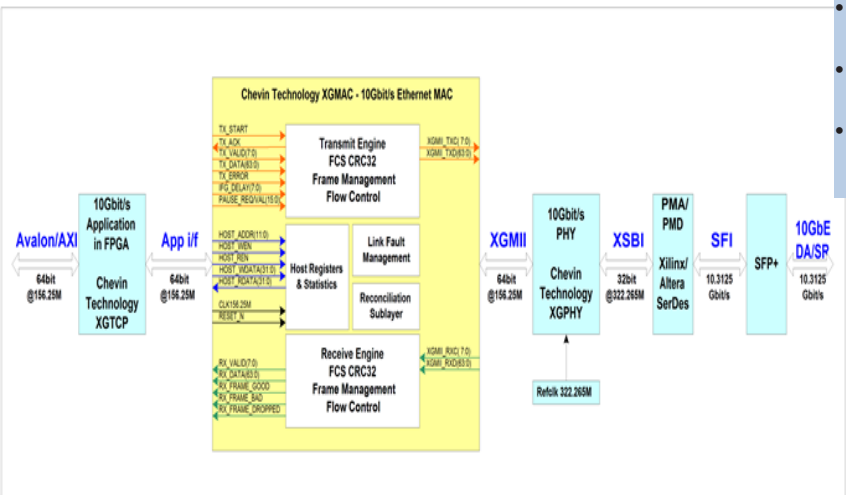
XGMAC (Cut-thru, no stats)	2700 LUTs
XGMAC (Cut-thru, with stats)	3000 LUTs
XGMAC (Store&Fwd, with stats)	2900 LUTs

Options

Statistics block	4 Block RAMs
Store&Forward	4 Block RAMs

Other Chevin Technology IP

- XGPHY – 10Gbit/s PCS 10G BASE-R
- XGTCP - 10Gbit/s TCP Server/Client
- XGUDP - 10Gbit/s UDP Server/Client.
- XGICMP/ARP – 10Gbit/s support library
- XGUDT4 – 10Gbit/s UDT4 Server
- SATAv3.2 – 1.5/3/6Gbit/s SSD Host Ctrl



CHEVIN TECHNOLOGY

Mentor Graphics

pads personal automated design system

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